AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (original) A clock signal generation circuit for generating multiphase clock signals in accordance with a master clock signal having a predetermined frequency, comprising:

a master DLL circuit section adapted to generate a first delay signal obtained by delaying the master clock signal by a first delay time and generate a first pulse signal having a pulse width of the first delay time in accordance with the master clock signal and the first delay signal;

a multiphase clock generation circuit section adapted to generate multiphase internal clock signals in accordance with the master clock signal and generate delay internal clock signals obtained by delaying the multiphase internal clock signals, respectively; and

a slave DLL circuit section constituted by slave DLL circuits each for delaying, by a second delay time, corresponding one of the delay internal clock signals generated by the multiphase clock generation circuit section, thereby outputting the delayed delay internal clock signals which form the multiphase clock signals,

wherein the master DLL circuit section generates a first control signal which is changed in voltage in accordance with the first pulse signal, and adjusts the first delay time to have a

first predetermined value in accordance with the generated first control signal, and

wherein each of the slave DLL circuits generates a second pulse signal having a pulse width of the second delay time, and generates a second control signal which is changed in voltage in accordance with the first and second pulse signals, and adjusts the second delay time to have a second predetermined value in accordance with the generated second control signal.

2. (original) The clock signal generation circuit according to claim 1, wherein the master DLL circuit section comprises:

a first variable delay circuit which is fed back with the first control signal and delays the master clock signal by the first delay time in accordance with the fed-back first control signal, and generates the first delay signal;

a first pulse signal generation circuit for generating the first pulse signal in accordance with the first delay signal and the master clock signal;

a first charge pump circuit for charging and discharging a first capacitor in accordance with the first pulse signal; and

a first low-pass filter for integrating a voltage at a high voltage side of the first capacitor and outputting the integrated voltage to be fed to the first variable delay circuit as the first control signal.

3. (currently amended) The clock signal generation circuit according to claim 1, wherein each of the slave DLL circuits comprises:

a second variable delay circuit which is fed back with the second control signal and delays the corresponding delay internal clock signal by the second delay time in accordance with the fed-back second control signal and outputting the delayed delay internal clock signal as the clock signal for forming the multiphase clock signals;

a second pulse signal generation circuit for generating the second pulse signal in accordance with the clock signal outputted from the second variable delay circuit, the corresponding internal clock signal and the master clock signal;

a second charge pump circuit for charging and discharging a second capacitor in accordance with the first and second pulse signals; and

a second low-pass filter for integrating a voltage at a high voltage side of the second capacitor and outputting the integrated voltage to the second variable delay circuit as the second control signal.

4. (currently amended) The clock signal generation circuit according to claim 2, wherein each of the slave DLL circuits comprises:

a second variable delay circuit which is fed back with the second control signal and delays the corresponding delay internal clock signal by the second delay time in accordance with the fed-

back second control signal and outputting the delayed delay internal clock signal as the clock signal for forming the multiphase clock signals;

a second pulse signal generation circuit for generating the second pulse signal in accordance with the clock signal outputted from the second variable delay circuit (31), the corresponding internal clock signal and the master clock signal;

a second charge pump circuit for charging and discharging a second capacitor in accordance with the first and second pulse signals; and

a second low-pass filter for integrating a voltage at a high voltage side of the second capacitor and outputting the integrated voltage to the second variable delay circuit as the second control signal.

5. (currently amended) The clock signal generation circuit according to claim 3, wherein the second charge pump circuit comprises:

the second capacitor;

a charge circuit for charging the second capacitor in accordance with the ~~first~~ second pulse signal; and

a discharge circuit for discharging the second capacitor in accordance with the ~~second~~ first pulse signal.

6. (original) The clock signal generation circuit according to claim 5, wherein the discharging circuit adjusts a

discharge current of the second capacitor in accordance with an externally supplied digital signal.

7. (original) The clock signal generation circuit according to claim 5, wherein the charge circuit adjusts a charge current of the second capacitor in accordance with an externally supplied digital signal.

Claims 8-9 (canceled)